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PATENT, TRADEMARK, COPYRIGHT AND RELATED INTELLECTUAL PROPERTY LAW

June 6, 2006

Attn: The Certificate of Correction Branch

Commissioner for Patents

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Re:

U.S. Patent No.:

6,972,790 B2

Issued:

December 6, 2005

Title:

HOST INTERFACE FOR IMAGING ARRAYS

Inventor:

Mark Suska

Our Docket No.:

33214

Sir:

This is a second request for a Certificate of Correction under 35 U.S.C. 254 to correct Patent Office printing errors in the above-identified patent. The first request was sent March 22, 2006. Enclosed herewith is the original Certificate of Correction dated May 30, 2006. The certificate should state either "Column 10, Claim 19, Line 2" or "Column 10, Line 13". Also enclosed is the proposed Certificate of Correction (Form No. PTO-1050) and documentation in support of the proposed corrections for consideration which were sent with the first request.

It is requested that a new Certificate of Correction be completed and mailed at an early date to the undersigned attorney of record.

Respectfully submitted,

Ву_

John P. Murtaugh, Reg. No. 34226

lend. Mentangt

JPM/ck

Enclosures: Form PTO/SB/44

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date indicated below.

John P. Murtaugh

Name of Attorney for Applicant(s)

6-6-06

Date

Signature of Atterney

UNITED STATES PATENT AND TRADEMARK OFFICE **CERTIFICATE OF CORRECTION**

PATENT NO.

: 6,972,790 B2

DATED

: December 6, 2005

INVENTOR(S) : Mark Suska

Page 1 of 1

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 10,

Line 2, after "claim", delete "16" and insert -- 15 --.

Thirtieth Day of May, 2006

Signed and Sealed this

JON W. DUDAS Director of the United States Patent and Trademark Office

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO.

6,972,790 B2

PAGE 1 OF 1

DATED

December 6, 2005

INVENTOR(S)

Mark Suska

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Claim 19

Line 2, after "claim", please delete "16" and insert therefor --15--.

MAILING ADDRESS OF SENDER: John P. Murtaugh

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PATENT NO. 6,972,790 B2

No. of additional copies

0

Re-numbered
Claim

(Currently amended) An integrated semiconductor imaging circuit as
claimed in claim 15 where the interface includes for use with an electronic processing system having a data bus comprising:

- an imaging array sensor having an array of sensing pixels and an array address generator integrated on a die; and
- an interface integrated on the die for receiving data from the imaging array sensor as determined by the imaging array sensor and adapted to transfer the data to the electronic processing system as determined by the electronic processing system, the interface including:
 - a memory for storing imaging array data and address signals at a rate determined by the imaging array sensor; and
 - a circuit for controlling the transfer of the data from the memory to the data bus at a rate determined by the electronic processing system.
- 17. (Previously presented) An integrated semiconductor imaging circuit as claimed in claim 16 wherein the memory includes a first-in first-out (FIFO) buffer.
- 18. (Previously presented) An integrated semiconductor imaging circuit as claimed in claim 17 which further includes a bus arbitration unit coupled to the circuit for controlling the transfer of the data.
- 19. (Previously presented) An integrated semiconductor imaging circuit as claimed in claim 17 which further includes a bus arbitration unit integrated on the die and coupled to the circuit for controlling the transfer of the data.

Re-numbered claim <20.

(Previously presented) An integrated semiconductor imaging circuit as claimed in claim 16 wherein the memory includes an addressable memory.